DR. LIYAQAT NAZIR

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OBJECTIVE

To work effectively in an organization and be able to deliver to the bottom-line so as to be an asset to the organization. To take a challenging and high performance-oriented role in the field of Engineering Sciences and implement the expertise and experience gained in this field and make a difference in whatever I do.

CURRENT STATUS

Presently working as Assistant Professor in the department of Electronics and Communication Engineering, Islamic University of Science and Technology.

EDUCATION

2018 — **Doctor of Philosophy** in the faculty of Engineering, from **National Institute of Technology Srinagar**, Hazratbal, Srinagar, with an overall "**A+**" grade
Thesis title: "**Efficient Block and Microarchitectural level solutions of Network-on-Chip targeting FPGA platforms**."
Area of Research: Reconfigurable Hardware.

2013 — **M. Tech** degree in **Communication and IT,** from **N.I.T**, Srinagar, with an overall "**B+**" grade
Thesis work: "High speed low power design of Flash ADC using TIQ technique."

2011 — **B. Tech** degree in **Electronics and Communication**, from **Islamic University of Science and Technology,** Awantipora, with an aggregate percentage of **84.3%.**
Project Work: "Design of a semi-converter drive using 8085 microprocessors and 8051 microcontrollers. Supervised by Dr. A. H. Bhat (Associate professor, Electrical Engineering, National Institute Of Technology.

2005 — **XII** from I.M.I, Srinagar, J & K Board of School Education with an aggregate percentage of **68%.**

2003 — **X** from H.E.I, Srinagar, J & K Board of School Education with an aggregate percentage of **70%.**

EXPERIENCE

- Worked as Lecture (Non substantive basis) in the department of Electronics and Communication Engineering, Institute of Technology, Zakura campus, University of Kashmir from November 2017 till November 2020

- Worked as Research Scholar (Doctoral degree) at NIT, Srinagar, J&K. from Sept 2013 to Jan. My research work is mainly aimed at providing efficient solutions for NoC targeting FPGA platforms.

- Worked as Assistant professor (Tenure basis) in IUST for the month of August and September 2013.

PUBLICATIONS & RESEARCH WORK.

"**Principles and Practices of Low Power High Speed TIQ Based Flash ADC**", Authorship: Single, Publisher: Lambert Academic publishing. ISSN/ISBN: 978-3-330-05608-4. Publisher: International

BOOKS

1. **Self-Timed Comparator Based Power Efficient High Speed Analog to Digital Converter, published in "official journal of the patent office" issue 17/2016, page no. 14997, dated: 22/04/2016.**

PATENTS/ INVENTIONS

JOURNAL PAPERS

1. **"An Efficient Realization of FIFO Buffers for NoC Routers using Technology Dependent Optimizations Targeting LUT based FPGAs", in Int. J. of Circuits and Architecture Design (IJCAD), Vol. 2, Nos. 3/4, 2016. ISSN:2051-7033(online),2051-7025(print), journal: peer reviewed, non UGC listed, Authorship: primary co-author, journal status: International, publisher: Inderscience publishers, publishing charges: non paid. Published online 6 February 2018.**

2. **"Realization of Efficient High Throughput Buffering Policies for Network on Chip Router," in International journal of Computer Network and Information Security (IJCNIS), Vol. 8, No. 7, Jul. 2016. ISSN: 2074-9090 (Print), 2074-9104 (Online), journal: peer reviewed, non UGC listed, Authorship: primary co-author, journal status: International, publisher: MECS-Publishers, publishing charges: non paid. 8 July 2016**

3. **"Technology Dependent Solutions for Buffering Policies of Network on Chip Targeting FPGA Platforms," in International Journal of**

Information Technology and Electrical Engineering (ITEE journal), volume 5, issue 5, October 2016. ISSN:2306708X, journal: peer reviewed, UGC listed, UGC journal no: 44995, Authorship: primary co-author, journal status: International, publisher: International Journal of Information Technology and Electrical Engineering, publishing charges: non paid. Vol. 7, No. 5, page 30-45 October 2018

4. **"A Comprehensive Survey on Packet and Circuit Switched NoC Routers" in the Journal of Emerging Technologies and Innovative Research, volume 6, issue 5, page 506-509 June 2019. ISSN: 23495162, journal: peer reviewed, UGC listed, UGC journal no: 63975, Authorship: primary co-author, journal status: International.**
5. **"Comparative Study between Control Channel Establishment and Blind Rendezvous in Cognitive Radio Networks" in the Journal of Emerging Technologies and Innovative Research, volume 6, issue 5, page 566-569 June 2019. ISSN: 23495162, journal: peer reviewed, UGC listed, UGC journal no: 63975, Authorship: primary co-author, journal status: International.**

6. **"DTMF based smart notice board system", in International Journal of Scientific and Research Publications, Volume 3, Issue 11, November 2013 ISSN 2250-3153**

CONFERENCE PAPERS

1. **"A 4 GS/s, 1.8 V Multiplexer Encoder Based Flash ADC using TIQ Technique," in proceedings of Ist International Conference on Signal Processing and Integrated Networks (SPIN), IEEE, amity university, Noida, U.P. Feb 2014. DOI : 10.1109/SPIN.2014.6776997, Pages: 458 – 463,Date of Conference:20-21 Feb. 2014**

2. **"Performance Analysis of Various scheduling algorithms using FPGA Platforms," in the proceedings of International Conference on VLSI systems, Architecture, Technology and Applications. (VLSI-SATA), IEEE , Amrita University, Bangluru, Jan 2015. DOI: 10.1109/VLSI-SATA.2015.7050477, Pages: 1 - 4,Year: 2015,Date of Conference: 8-10 Jan. 2015**

3. **"Performance Evaluation of Different Allocation algorithms using FPGA Platforms," in proceedings of International Conference on Electronics and Communication Systems (ICECS'15), Feb 2015. DOI: 10.1109/ECS.2015.7125020, Pages: 792 - 795, Year: 2015,Date of Conference: 26-27 Feb. 2015**

4. **"FPGA Evaluation of Wave Front Allocator for crossbar based on-chip switches," in proceedings of International Conference on Advances in Computers, Communication and Electronic**

Engineering 2015,ISBN:9789382288541, Publication date: 16/03/2015

5. **"A 7GS/s, 1.2 V. Pseudo logic Encoder based Flash ADC Using TIQ Technique," in proceedings of 12th IEEE India International Conference Electronics, Energy, Environment, Communication, Computer, Control, (E3-C3) 2015 (IEEE INDICON 2015), Jamia Millia Islamia, New Delhi, INDIA. ISSN: 2325-9418,DOI: 10.1109/INDICON.2015.7443459, Pages: 1 - 6, Year: 2015,Date of Conference: 17-20 Dec. 2015**

6. **"A 4.5 GS/S, 1.2 V Domino logic Encoder based Flash ADC using TIQ Technique," in proceedings of 2nd International Conference on Signal processing and integrated networks (SPIN2015). ISSN: 2325-9418, Date of Conference: 20 Feb 2015**

7. **"Implementation of X-Y Routing Algorithm for NoC on Reconfigurable Platforms," Third International Conference on Nanotechnology for Better Living, May 25-29, 2016.vol 3, No. 1, p. 215 DOI: 10.3850/978-981-09-7519-7nbl16-rps-215**

8. **"FPGA inbuild Macro Based Optimised Realisation of Round Robin Arbiter", IEEE Sponsored International Conference on Innovations in Information, Embedded And Communication Systems (ICIIECS 17). 17-18th March 2017**
9. **"Evaluation of efficient elastic buffers for network on chip router", in the proceedings of IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI), Page s: 2176 – 2180, 2017, DOI: 10.1109/ICPCSI.2017.8392105, Pages: 2176 - 2180, Year: 2017,Date of Conference: 21-22 Sept. 2017**
10. **"Technology optimized fixed-point bit-parallel multiplier for LUT based FPGAs", in the proceedings of 2nd International Conference on Electronics and Communication Systems (ICECS),2015,ISBN:978-1-4799-7225-8DOI: 10.1109/ECS.2015.7124915, Pages: 316 - 321, Year: 2015, Date of Conference: 26-27 Feb. 2015**
11. **"An Efficient, Reliable FM based Campus Notification Dissemination System" in the proceedings of Advanced Research in Electrical and Electronic Engineering p-ISSN: 2349-5804; e-ISSN: 2349-5812 Volume 6, Issue 2 April-June, 2019, pp. 56-61 (Krishi Sanskriti Publications).**
12. **"Efficient Thought-Controlled Automation System for Differently Abled Persons" in the proceedings of Advanced Research in Electrical and Electronic Engineering p-ISSN: 2349-5804; e-ISSN: 2349-5812 Volume 6, Issue 2 April-June, 2019, pp. 62-64 (Krishi Sanskriti Publications)**

UG Courses Taught:	Analog Electronics-I, Analog Electronics –II, Basic Electronics, Data Communication, Microprocessors (8085), Mechatronic Systems,
PG level Lab conducted (During Ph.D.)	VLSI Design, VLSI DSP core, Advanced computer architecture, Mixed signal design
PROFESSIONAL COUSE WORK OPTED	Digital VLSI Design, Advanced VLSI Core, Digital System Design, Interconnection Networks, Advanced Computer architecture, Mixed signal Design, Analog VLSI design, Physics of Semiconductor devices, Embedded system design, Digital communication.
PROFESSIONAL WORKSHOPS CONDUCTED	• Conducted two week workshop on "**Research Write up with Latex** " from 1 February 2018 to 14 February 2018 at IOT, University of Kashmir.
PROFESSIONAL TRAINING/ WORKSHOPS/ SHORT-TERM COURSES/ CONFRENCES ATTENDED	• Ten-day workshop on **"Training Program on Big Data Analytics"** held from 10th to 20th March 2017, at NIT Srinagar. • Participated in AICTE recognized one week short term course on "**Open Source Technologies through ICT**" organized by NITTTR Chandigarh held from 04th January 2016, at NIT Srinagar. • 40 hour training program on **"VLSI Design,"** organized by resolute consultancy at IUST on Nov 2009. • Participated and presented a paper in "**National Research Scholars Conclave on Innovation and Recent Trends in Science and Technology"** held on 02-03 April 2016, at NIT Srinagar. • Participated in **Digital India Week 2015** organized by Department of Electronics and Information Technology in collaboration with NIT Srinagar. • Participated in "**Diamond Jubilee Seminar on Leveraging ICT for Growth and Development of J&K**" held on 13-14 September 2013, at NIT Srinagar. • One day workshop on **"National Mission on Education through**

Information Communication Technology (NME-ICT).” held on 18 June 2013, at NIT Srinagar.

- Six day 27th international conference on **"VLSI Design,"** held in Indian Institute of Technology Bombay (IITB) from 5th to 10th Jan 2014.
- Participated in Ist **International Conference on Signal Processing and Integrated Networks (SPIN), IEEE**, held on 20th-21th Feb. 2014, at Amity University, noida, U.P.
- Attended one day tutorial in **International Conference on VLSI systems, Architecture, Technology and Applications. (VLSI-SATA),** IEEE, Amrita University, Bangalore, Jan 2015.
- Participated in **International Conference on VLSI systems, Architecture, Technology and Applications. (VLSI-SATA).** Jan 2015.
- Participated in One day tutorial in **International Conference on VLSI systems, Architecture, Technology and Applications. (VLSI-SATA),** Bangalore, Jan 2015.
- Six weeks training on “**Hydro power generation and distribution,”** from 25/11/2010 to 07/01/2011 at JKPDC, Ganderbal hydro power generation division.

MEMBERSHIP RESEARCH BODIES

1. Member of **Institute of Electrical and Electronics Engineers (IEEE) since 2013.**
2. Associate Member of the **Institution of Electronics and Telecommunication Engineers (IETE),** New Delhi.

RESEARCH INTERESTS

- Low power mixed signal design.
- VLSI System Design
- Network on Chip.
- Reconfigurable design (FPGA).
- Interconnection Networks

COMPUTER SKILLS

Programming: C, VHDL, HTML, System C, Latex, Python
Research Document type setting: Latex
Simulation tools: Matlab, Xilinx ISE, Vivado, Advanced design systems

(ADS), Cadence Virtuso, Pspice, Altera Quartus, KiCAD.
Applications: MS Word, MS Excel, MS power point, Bibtex .
Statistical tools and Drawing tools: SPSS (IBM statistical tool), Minitab, Origin.
Drawing tools: Microsoft Visio, Dia.
Platforms: Windows, Linux.

ADDRESS

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Date: 17-11-2020. **LIYAQAT NAZIR**