Semester-V

Course Code	Course Title	L – P	Credit
CSE-511T	Design and Analysis of Algorithms	4 – 0	4
CSE-512T	Operating System	4 – 0	4
CSE-513T	Microprocessors, Peripherals and Interfacing	4 – 0	4
CSE-514T	Computer Networks	4 – 0	4
CSE-515T	Computer Architecture and Organization	4 – 0	4
XXX-ExxX	Elective-III		X
CSE-516P	Design and Analysis of Algorithms Lab	0 – 2	1
CSE-517P	Microprocessors, Peripherals and Interfacing Lab	0 – 2	1
CSE-518P	Computer Networks Lab	0 – 2	1
	Total Credits	**20 – 6**	**23+X**

Design and Analysis of Algorithms
CSE-511T

L	P
4	0

Unit-I

Introduction: Algorithm Design paradigms- motivation, concept of algorithmic efficiency, run time analysis of algorithms, Asymptomatic Notations.

Divide & Conquer: Structure of divide and conquer algorithms: examples, Binary search, Quick sort, analysis of divide and conquer run time reference relations.

Unit-II

Greedy method: Overview of the greedy paradigm, examples of exact optimization solution (minimum cost spanning tree), approximate solution (Knapsack problem), single source shortest paths.

Dynamic Programming: Overview, difference between dynamic programming and divide and conquer, applications: shortest path in graph, matrix multiplication, travelling salesman problem, longest common sequence.

Unit-III

Graph searching and traversal: Overview, traversal methods, depth first and breadth first search. Dijkstra's and Bellman Fort Algorithm for finding Single source shortest paths. All pair shortest paths and matrix multiplication, Floyd – Warshall algorithm for all pair shortest paths.

Unit-IV

Back Tracking: Overview, 8-queen problem and Knapsack problem.

Branch & Bound: LC searching, bounding, FIFO branch and bound, Applications: 0/1 Knapsack problem, Travelling salesman problem.

Unit-V

String matching: The naïve String Matching algorithm, The Rabin-Karp Algorithm, The Knuth-Morris Pratt algorithm.

Computational complexity: Complexity measures, Polynomial vs non-polynomial time complexity; NP hard and NP complete classes, examples

Books Recommended:

1. T. H. Cormen, C. E. Leiserson, R. L. Rivest, Clifford Stein, "Introduction to Algorithms", 2nd Ed., PHI, 2004.

References Books:

1. Ellis Horowitz and Sartaz Sahani, "Computer Algorithms", Galgotia Publications, 1999.
2. V. Aho, J. E. Hopcroft, J. D. Ullman, "The Design and Analysis of Computer Algorithms", Addition Wesley, 1998.
3. D. E. Knuth, "The Art of Computer Programming", 2nd Ed., Addison Wesley, 1998.

Operating System
CSE-512T

L	P
4	0

UNIT I
Computer System Overview-Basic Elements, Instruction Execution, Operating system functions and structure, Interrupts, Memory Hierarchy, Cache Memory, Direct Memory Access, Multiprocessor and Multicore Organization. Operating system overview-objectives and functions, Evolution of Operating System, Distributed OS.

UNIT II
Process concept, Process States, Process Description and Process Control, Interprocess Communication, Processes and Threads, Types of Threads, Multicore and Multithreading,

UNIT III
Principles of Concurrency - Mutual Exclusion, Semaphores, Monitors, Readers/Writers problem. Deadlocks – prevention- avoidance – detection, Scheduling- Types of Scheduling – Scheduling algorithms.

UNIT IV
Memory management requirements, Partitioning, Paging and Segmentation, Virtual memory - Hardware and control structures, operating system software, Linux memory management, Windows memory management. Virtual memory management.

UNIT V
I/O management and disk scheduling – I/O devices, organization of I/O functions; OS design issues, I/O buffering, disk scheduling, RAID, Disk cache. File management – Organization, Directories, File sharing, and Record blocking, secondary storage management.

Text Books:

1. Silberschatz, Peter Galvin, Greg gagne "Operating System Principles".

Reference Books:

1. Andrew S. Tannenbaum & Albert S. Woodhull, "Operating System Design and Implementation", Prentice Hall.
2. William Stallings, "Operating Systems – internals and design principles", Prentice Hall.
3. Andrew S. Tannenbaum, "Modern Operating Systems", Prentice Hall.
4. Gary J.Nutt, "Operating Systems", Pearson/Addison Wesley.
5. Pramod Chandra P.Bhatt, "An Introduction to Operating Systems Concepts and Practice".

Microprocessors, Peripherals and Interfacing
CSE-513T

L	P
4	0

UNIT-I

Introduction To 8-bit Microprocessor: History of Microprocessor, 8085 Microprocessor architecture, buses, register, flags. 8085 pin configuration & function of each pin. Fetch, Decode and execute operations. Op-code Fetch, execute cycle, T state, Machine cycle. Memory and I/O read and write cycles WAIT state, interrupt timing diagram.

UNIT-II

Intel 8085 Microprocessor Instruction Set and Programming: Addressing modes of 8085. Data transfer, Arithmetic, Logical, Rotate, Branch and machine control instructions. Development of 8085 assembly language programs, time delays. Concept of stack and Instruction related to stack. 8085 interrupts, RST, RIM, SIM instructions. Subroutines and conditional call instruction

UNIT-III

Interfacing of Memory Chips & Input / Output Chips: Memory mapped I/o and I/O mapped I/O. Address decoding, interfacing of memory chips with 8085. Interfacing of input/output chips with 8085

UNIT-IV

Peripherals IC and Applications: Block diagram, Pin description and Interfacing of 8255(PPI) with 8085 Microprocessor. Interfacing of keyboard, display, ADC and DAC to 8255. Block diagram, Pin description and Interfacing of 8253(PIT) with 8085 Microprocessor. Brief description and application of 8259 PIC, 8251 USART and 8237 DMA Controller

UNIT-V

Introduction advance Microprocessor: Intel 8086 Microprocessor architecture, Addressing Modes, 8086 pin configuration & function of each pin. Introduction and advance features of 8088, 80186, 80286, 80386 and 80486microprocessor

RECOMMENDED BOOKS:

1. Microprocessor Architecture, Programming, and Applications with the 8085 –Ramesh S. Gaonkar Pub: Penram International.
2. Microprocessor 8085 and its Interfacing, By Sunil Mathur, Second Edition, PHI Learning Pvt. Ltd.
3. 8085 Microprocessor And its Applications, By A. Nagoor Kani, Third Edition,TMH Education Pvt. Ltd
4. Microprocessors and interfacing - Douglas V. Hall, TMH, 2nd Edition, 1999.

Computer Networks
CSE-514T

L	P
4	0

Unit I

Introduction: Uses of Computer Networks, Network and Protocol Architecture, Reference Model (ISO-OSI, TCP/IP-Overview).

UNIT-II

Data Link layer – Design Issues, Error detection and Correction, Elementary and sliding Window data link protocols, Data link layer in HDLC, Point to Point protocol ALOHA, carrier sense multiple access, collision free protocols, IEEE standards –802.3, 802.4, 802.5: Transparent and source routing bridges.

UNIT-III

Network Layer: IP Addressing, IPv.4 Vs IPv.6, Class C Subnetting, virtual circuit and datagram subnets – Routing algorithm shortest path routing, Flooding, Hierarchical routing, Broad-cast, multicast, distance vector routing. Congestion control Algorithms – General principles of congestion prevention policies.

UNIT-IV

Internet working: The Network layer in the Internet.

Transport Layer: Transport services, Elements of Transport protocols, Internet Transport

Protocols. TCP, UDP, TCP sockets

UNIT-V

Application Layer-Network Security: Domain Name system: Electronic Mail; The world

Wide Web; DHCP;

TEXT BOOKS:

1. W. Stallings, "Computer Communication Networks", PHI, 1999.
2. Larry L.Peterson, Peter S. Davie, "*Computer Networks*", Elsevier, Fifth Edition, 2012.
3. Computer Networks – Third Edition – Andrew S. Tanenbaum, Prentice Hall of India.
4. Data Communications and Networking – Behrouz A. Forouzan.Third Edition TMH.

References:

1. U. Black, "Computer Networks-Protocols, Standards and Interfaces", PHI, 1996.
2. Laura Chappell, "Introduction to Cisco Router Configuration", Techmedia, 1999.
3. Michael A. Miller, "Data & Network Communications", Vikas Publication, 1998.
4. William A. Shay, "Understanding Data Communications & Networks", Vikas Publication, 1999.

Computer Architecture and Organization
CSE-515T

L – P
4 - 0

Unit-I:
Register Transfer and Micro-operations
Register Transfer Language, Register Transfer, Bus and Memory Transfers, Arithmetic Micro-operations, Logic Micro-operations, Shift Micro-operations, Arithmetic Logic Shift Unit, Instruction Codes, Computer Registers, Computer Instructions, Timing and Control, Instruction Cycle, Memory-Reference Instructions, Input-Output and Interrupt, Complete
Computer Description. Control Memory, Address Sequencing, Micro program Example.

Unit-II: Design of Control Unit
Hardware and Software Control Unit, single Bus artecture
Unit-III: Input-Output Organization
Peripheral Devices, Input-Output Interface, Asynchronous Data Transfer, Modes of Transfer, Priority Interrupt, Direct Memory Access, I/O Controller

Unit-IV: Memory Organization -
Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Virtual Memory.

Unit-V: Arithmetic -
Addition and Subtraction of Signed Numbers, Addition/Subtraction Logic Unit, Design of Fast Adders, Carry Lookahead Addition, Multiplication of Positive Numbers, Signed Operand Multiplication, Booth Algorithm, Integer Division, IEEE Standard for floating point numbers.

Text Books:

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky, "Computer Organization", McGraw-Hill, Fifth Edition, Reprint 2012.

Recommended Books:

1. Ghosh T. K., "Computer Organization and Architecture", Tata McGraw-Hill, Third Edition, 2011.
2. W. Stallings, "Computer Organization & Architecture", PHI.
3. J. P. Hayes, "Computer Architecture and Organization", McGraw Hill
4. J. L Hennessy and D. A. Patterson, "Computer Architecture: A quantitative approach", Morgon Kauffman, 1992.
5. Computer Systems Organization and Architecture, John D. Carpinelli, Pearson Education Inc.

Design and Analysis of Algorithms Lab
CSE-516P

L	P
0	2

Lab Details:

The Following Problems Are To Be Solved In C

Simple Experiments on time and space complexity of a program

Divide and Conquer Approach: Merge Sort, Quick sort, Medians and Order statistics, Strassen's algorithm for Matrix Multiplications.

Greedy Algorithms: Knap Sack Problem, An activity selection problem, Huffman Codes, A task scheduling problem.

Dynamic Programming: Matrix Chain Multiplication, Longest common subsequence and optimal binary search trees problems.

Graph Algorithms: Representation of Graphs, Breadth First Search, Depth First Search, Topological Sort, Strongly Connected Components, Algorithm for Kruskal's and Prim's for finding Minimum cost Spanning Trees, Dijkstra's and Bellman Fort Algorithm for finding Single source shortest paths. All pair shortest paths and matrix multiplication, Floyd – Warshall algorithm for all pair shortest paths.

Back Tracking: 8-queen problem and Knapsack problem.

Branch & Bound: LC searching, bounding, FIFO branch and bound,

String matching: The naïve String Matching algorithm, The Rabin-Karp Algorithm, The Knuth-Morris Pratt algorithm.

Microprocessors, Peripherals & Interfacing lab
CSE-517P

L	P
0	2

Lab Details:

1. To develop a program to add two double byte numbers.
2. To develop a subroutine to add two floating point quantities.
3. To develop program to multiply two single byte unsigned numbers, giving a 16 bit product.
4. To develop subroutine which will multiply two positive floating point numbers.
5. To write program to evaluate P* Q*+R* & S are 8 bit binary numbers.
6. To write a program to divide a 4 byte number by another 4 byte number.
7. To write a program to divide an 8 bit number by another 8 bit number upto a fractional quotient of 16 bit.
8. Write a program for adding first N natural numbers and store the results in memory location X.
9. Write a program which decrements a hex number stored in register C. The Program should half when the program register reads zero.
10. Write a program to introduce a time delay of 100 ms using this program as a subroutine display numbers from 01H to OAH with the above calculated time delay between every two numbers.
11. N hex numbers are stored at consecutive memory locations starting from X. Find the largest number and store it at location Y.
12. Interface a display circuit with the microprocessor either directly with the bus or by using I/O ports. Write a programme by which the data stored in a RAM table is displayed.
13. To design and interface a circuit to read data from an A/D converter, using the 8255 A in the memory mapped I/O.
14. To design and interface a circuit to convert digital data into analog signal using the 8255 A in the memory mapped I/O.
15. To interface a keyboard with the microprocessor using 8279 chip and transfer the output to the printer.
16. To design a circuit to interface a memory chip with microprocessor with given memory map.

Computer Network Lab
CSE-518P

L – P
0 - 2

Lab Details:

1. Identification of guided media (UTP,Fibre) /Color coding.
2. To Connect two pc using peer to peer communication/via switch/via router.
3. IP addressing (static and dynamic).
4. Sharing the resources in wired network (software and hardware).
5. Configuring the Windows server (Active directory) and DHCP server.
6. Study of NS2/ GLOMOSIM / OPNET.
7. To implement wired network topology and wireless network topology in NS2.